MODIFIED GLITCH LATCH FOR USE WITH POWER SAVING DYNAMIC REGISTER FILE STRUCTURES

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ABSTRACT OF THE DISCLOSURE

In the Retirement Payload Array (RPA) of a microprocessor, the signal "READ" is logically combined with the primary clock signal "CLK" in a control circuit of a modified glitch latch such that the glitch latch will only reset, and therefore a reset edge or "glitch" will only appear, when new data is read and the signal IN will return to zero and allow the modified glitch latch to recover.